20.3 A Wireless Transceiver with Integrated Data Converters for 802.11a/b/g Access Points

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In order to keep client costs and power dissipation low, it is desirable for 802.11a/b/g access points (APs) to exceed the minimum performance requirements set forth by the standard. For example, an AP with improved sensitivity allows a link to be established at a lower client transmit power. Furthermore, a high performance AP can improve network throughput since the SNR determines the selection of the data rate. For example, if a receiver can tolerate a 6dB lower SNR, its data rate can be increased by more than a factor of two. Alternatively, the same SNR-requirement reduction can result in a free-space range improvement by a similar factor. The transceiver described in this paper optimizes AP performance by supporting maximum-ratio combine (MRC) diversity on the receive side and by maximizing output power while minimizing EVM on the transmit side.

The block diagram of the IC is shown in Fig. 20.3.1. Included in the block diagram are the RF transceivers, baseband data converters, some digital signal conditioning, and a high-speed serial link for communication with the baseband processor. The advantage of this partition over the SoC approach [1] is that the elimination of analog circuitry from the baseband processor can result in cost and power dissipation savings since migration to the latest technology node is greatly simplified for an all-digital IC. Further, the testing of an all-digital IC can be significantly less costly than that of one with analog or RF content. An advantage over the analog-IQ partition [2] is that the inclusion of the converters on the same die as the transceiver allows real-time functions such as AGC, transmit power control (TPC), and signal detection to be autonomous. The reduced real-time software requirement can result in a shorter time-to-market.

Referring again to Fig. 20.3.1, the LO path consists of a single VCO that is locked to a 40MHz reference frequency by a ΔΣ fractional-N synthesizer. The high-band (4.9 to 5.9GHz) LO is generated by mixing the VCO output with the same signal divided by two and rejecting undesired mixing products with an LC tank. Accurate quadrature is ensured by passing the resulting signal through a polyphase filter before a final phase of amplification/buffering (not shown). The low-band (2.3 to 2.7GHz) LO is similarly generated except the VCO output is mixed with itself divided by four instead of two. The minimum frequency step is 1MHz in both bands.

The receivers use conventional direct-conversion topologies with 75dB maximum voltage gain and 72dB of gain control in 3dB steps. Two 12dB gain steps are applied at the LNA. Following the mixer and VGA, a 3rd-order, 14MHz lowpass filter attenuates alternate channel interference and provides 0 to 24dB of gain in 6dB steps. The baseband I and Q signals are then digitized by 160MS/s, 3rd-order, 5b CT ΔΣ ADCs. The ΔΣ ADCs have a lowpass signal transfer function with 3dB frequency of 26MHz, and zeros at multiples of 160MHz which provides inherent alias rejection and further attenuation of interferers. A decimation filter at the ADC output provides the final stage of interference rejection and produces 40MS/s 12b output data. The AGC loop is completely integrated and autonomous. Energy detect (ED) thresholds are user programmable. If the signal power in the selected channel is above the ED threshold, a control data packet is sent over the serial link to alert the modem of the presence of a signal. DC-offset compensation DACs (not shown for simplicity) inject current into the downconverter outputs and are controlled by an autonomous loop.

Figure 20.3.2 is a simplified schematic of the IC in which the transmit path and the TPC loop are emphasized. The direct-conversion transmitter has 44.875dB power control range with 27dB applied at the RF driver amplifier, 15dB applied at the upconverter, and 2.875dB applied in the digital baseband in 0.125dB steps. The RF VGA consists of parallel cascode stages with W/L weighting such that grounding the gates of groups of common-gate devices results in 3dB gain steps. This gain-control approach has the dual benefit of power dissipation that scales with output power and a relatively constant input capacitance which is important because the mixer is loaded by an LC tank. Oxide breakdown is avoided by adding a transistor with its gate connected to V_{DD} in series with the gain-control switch. The 12b baseband transmit data enters the chip at 40MS/s via the serial link and is upsampled to 160MS/s before being converted to the analog domain via the DACs.

The power detected at the output of the PA is converted to baseband via a downconverter that is optimized to have a temperature and frequency independent gain. Accurate gain is relatively easy to achieve since the received signal is large. The degenerated common-source input amplifier is loaded with very small resistors resulting in a very wide bandwidth. Both the input amplifier and downconverter are biased such that $g_m \propto 1/R$ resulting in a process and temperature independent gain.

After down-conversion, the signal is amplified and digitized via the receive baseband path which would otherwise be idle in transmit mode. The dc offset is cancelled and the signal power is measured in the digital domain. The measured power is compared to a reference that is scaled by the user-entered transmit attenuation setting (TXAtten) and a new transmit gain that minimizes the difference between the actual and desired power is calculated digitally. Transmit power errors measured during one burst are corrected on subsequent bursts. The detector path is only active during the preamble which is typically very short compared to the active part of the burst; consequently, the average power consumed is nearly zero.

Figure 20.3.3 shows the receiver EVM versus input power using a 54Mb/s 802.11a/g signal. The superior EVM floor exhibited by the low band is a result of the roughly 6dB better LO phase noise in that band. Figure 20.3.4 shows the RX sensitivity at 54Mb/s with and without diversity enabled when coupled to a companion modem IC. The diversity feature improves sensitivity by 2.5dB with a static channel. Sensitivity improvements are much larger in a multi-path environment.

Figure 20.3.5 shows the transmit output power and EVM versus the transmit attenuation setting. Note that the error in the transmit output power is less than ±0.5dB over a 40dB range and the EVM is less than -35dB over most of the range. The EVM degradation at low output power is due to the noise added by the test equipment.

A summary of the measured performance is shown in Figure 20.3.6. The 25mm^2 die – shown in Figure 20.3.7 - is manufactured in a 0.18μm CMOS.

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References:
[1] S. Mehta et al., "An 802.11g WLAN SoC", *ISSCC Dig. Tech. Papers,* pp. 94-95, Feb., 2005.
[2] A. Behzad et al., "Direct-Conversion CMOS Transceiver with Automatic Frequency Control for 802.11a wireless LANs", *ISSCC Dig. Tech. Papers,* pp. 356-357, Feb., 2003.

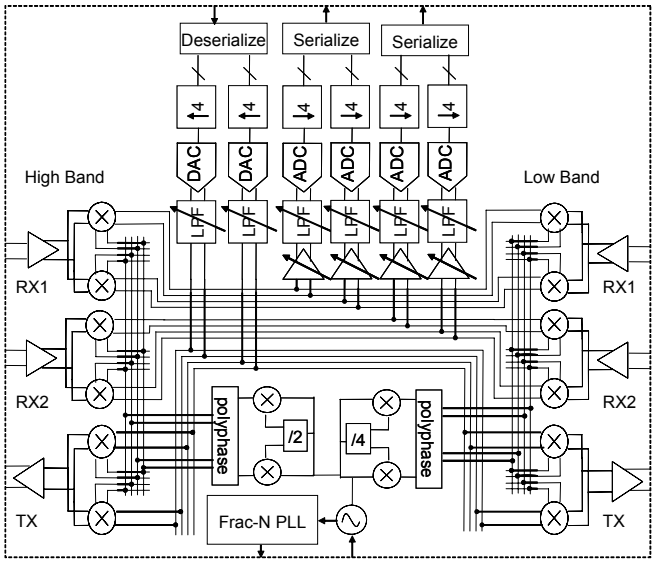

Figure 20.3.1: Block diagram of the transceiver.

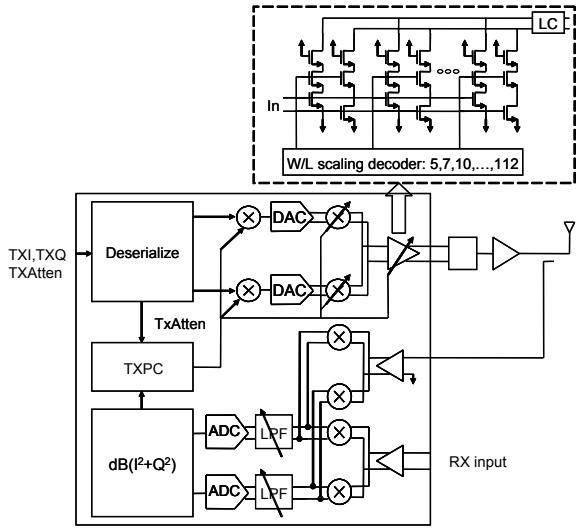

Figure 20.3.2: Block diagram emphasizing the transmit path and the closed-loop transmit power control.

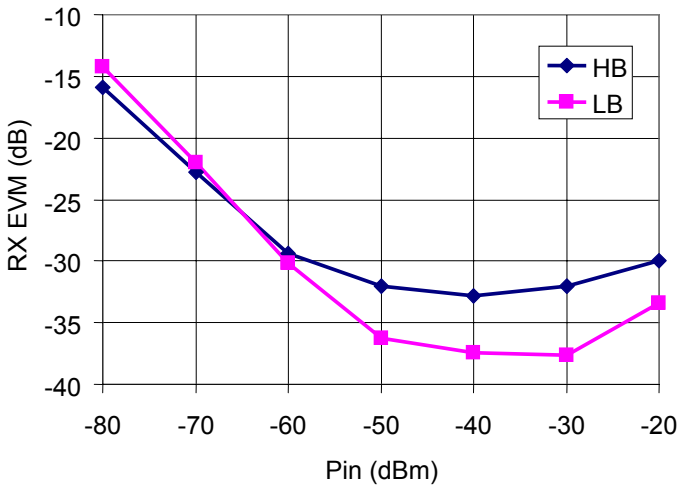

Figure 20.3.3: Receive EVM versus input power.

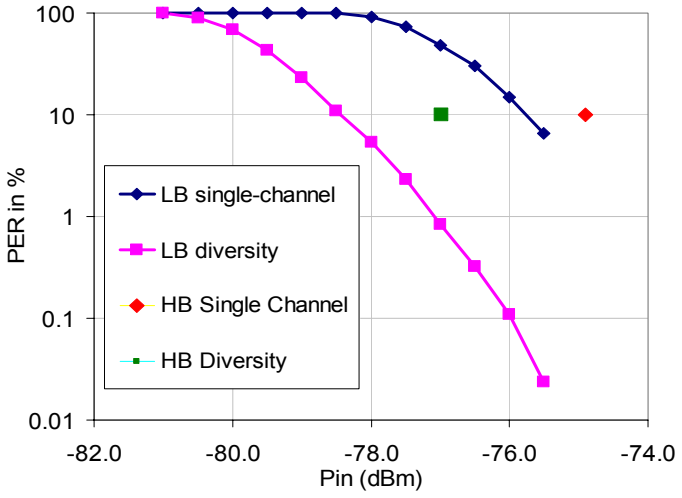

Figure 20.3.4: Packet error rate versus input power with and without diversity enabled.

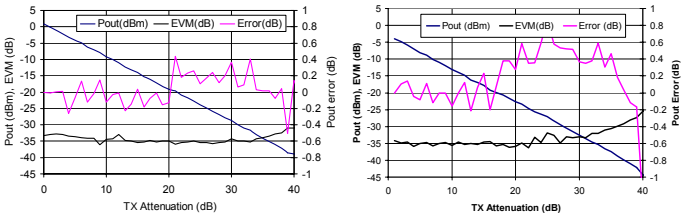

Figure 20.3.5: Transmit performance.

	Low band	High band
Supported bands (GHz)	2.3-2.7	4.9-5.9
RX NF dB (max gain)	3.9	4.2
LO phase noise (°rms)	0.33	0.75
TX Pout, EVM < -30dB (dBm)	3.7	-0.6
TX EVM @ -5 dBm (dB)	-35	-35
TX power consumption (W @ 3.3V)	0.9	1
RX power consumption, non-diversity (W @ 3.3V)	0.9	1.1
RX power consumption, diversity (W @ 3.3V)	1.6	1.7
Technology	0.18µm 1P6M CMOS	

Figure 20.3.6: Performance summary.

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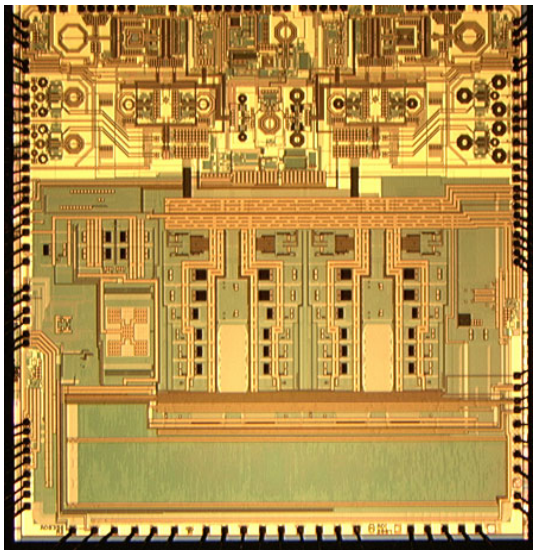

Figure 20.3.7: Die micrograph.

